CLAIMS

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1. In a video encoding system including a video source providing multiple frame video signal, a memory unit, , a compressed data interface, a host interface and a video encoding device, connected to the video source, the memory unit and the host interface, the video encoding device comprising:

a video input processor, for receiving said video signal,

a global controller, for controlling the global operation of said video encoding device, connected to said video input processor,

a motion estimation processor, connected to said global controller,

a digital signal processor, connected to said global controller and said motion estimation processor, and

a bit-stream processor connected to said digital signal processor and said global controller and said compressed data interface,

said global controller stores encoding commands received from said host interface thereby programming said video input processor, said motion estimation processor, said digital signal processor and said bit-stream processor,

said video input processor receiving and storing said video signal in said memory unit,

said motion estimation processor retrieving said video signal from said memory unit, generating motion analysis of said video signal, storing said motion analysis in said memory unit and providing said motion analysis to said digital signal processor,

said digital signal processor processing said video signal according to said motion analysis, thereby producing an encoding commands sequence and encoded data,

said bit-stream processor producing an encoded video signal according to said encoding command sequence and said encoded data.

2. The video encoding device according to claim 1, wherein at least one of said video input processor, said motion estimation processor, said digital signal processor and said bit-stream processor is directly connected to said memory unit.

3. The video encoding device according to claim 1, wherein at least one of said video input processor, said motion estimation processor, said digital signal processor and said bit-stream processor is connected to said memory unit via said global controller.

4. The video encoding device according to claim 1, wherein said motion estimation processor, said digital signal processor and said bit-stream processor operate in parallel.

5. The video encoding device according to claim 4, wherein said motion estimation processor operates on a macro-block i, said digital signal processor operates on a macro-block j and said bit-stream processor operates on a macro-block k, wherein i>j>k.

6. The video encoding device according to claim 1 wherein said video encoding device is entirely constructed on a monolithic semiconductor.

BI CONCL

7. A motion estimation processor comprising a controller and a plurality of resolution processors, connected to said controller,

said plurality of resolution processors analyzing the development of said video signal in time, thereby producing motion analysis,

said controller controlling said plurality of resolution processors.

8. The motion estimation processor according to claim 7 wherein said plurality of resolution processors include at least one low resolution processor, for producing low resolution motion analysis.

9. The motion estimation processor according to claim 7 wherein said plurality of resolution processors include at least one full resolution processor for producing full resolution motion analysis.

10. The motion estimation processor according to claim 7 wherein said plurality of resolution processors include at least one hyper resolution processor for producing hyper resolution motion analysis.

11. The motion estimation processor according to claim 8 wherein said at least one low resolution processor reduces the resolution of a selected frame before producing said low motion analysis.

12. The motion estimation processor according to claim 10 wherein said at least one hyper resolution processor enhances the resolution of a selected frame before producing said hyper resolution motion analysis.

13. The motion estimation processor according to claim 11 said wherein plurality of resolution processors include at least one full resolution processor for producing full resolution motion analysis.

14. The motion estimation processor according to claim 9 wherein said plurality of resolution processors include at least one hyper resolution processor, for producing hyper resolution motion analysis.

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15. A digital signal processor for processing a multiple frame video digital signal, comprising:

a DSP controller,

a plurality of processing units connected to said DSP controller for processing said multiple frame video digital signal; and

at least one storage unit, wherein each of said processing units is connected to at least one of said at least one storage units,

said DSP controller controlling said plurality of processing units.

16. The digital signal processor according to claim 15 wherein each of said processing units is operative to access any storage address of any of said at least one storage unit, connected thereto.

17. The digital signal processor according to claim 15 wherein each of said processing units operates according to a different program command.

18. The digital signal processor according to claim 15 wherein each of said processing units operates on a different portion of data.

19. A video camera comprising:

an optical assembly,

a light sensitive device, detecting light via said optical assembly, thereby producing video signal

a compressed data interface,

a memory unit, and

a video encoding device, connected to said light sensitive device,

said video encoding device comprising

a video input processor, for receiving said video signal,

a global controller, for controlling the global operation of said video encoding device, connected to said video input processor,

a motion estimation processor, connected to said global controller,

a digital signal processor, connected to said global controller and said motion estimation processor, and

a bit-stream processor connected to said digital signal processor and said global controller and said compressed data interface,

said video input processor receiving and storing said video signal in said memory unit,

said motion estimation processor retrieving said video signal from said memory unit, generating motion analysis of said video signal, storing said motion analysis in said memory unit and providing said motion analysis to said digital signal processor,

said digital signal processor processing said video signal according to said motion analysis, thereby producing an encoding commands sequence and encoded data,

said bit-stream processor producing an encoded video signal according to said encoding command sequence and said encoded data.

said global controller stores encoding commands received from said host interface thereby programming said video input processor, said

motion estimation processor, said digital signal processor and said bit-stream processor,

20. The video encoding device according to claim 1 wherein said motion estimation processor comprises a controller and a plurality of resolution processors, connected to said controller,

said plurality of resolution processors analyzing the development of said video signal in time thereby producing motion analysis,

said controller controlling said plurality of resolution processors.

21. The video encoding device according to claim 20 wherein said plurality of resolution processors include at least one low resolution processor for producing low resolution motion analysis.

22. The video encoding device according to claim 20 wherein said plurality of resolution processors include at least one full resolution processor for producing full resolution motion analysis.

23. The video encoding device according to claim 20 wherein said plurality of resolution processors include at least one hyper resolution processor for producing hyper resolution motion analysis.

24. The motion estimation processor according to claim 21 wherein said least one low resolution processor reduces the resolution of a selected frame before producing said low motion analysis.

25. The motion estimation processor according to claim 23 wherein said least one hyper resolution processor enhances the resolution of a selected frame before producing said hyper resolution motion analysis.

26. The motion estimation processor according to claim 24 wherein said plurality of resolution processors include at least one full resolution processor for producing full resolution motion analysis.

27. The motion estimation processor according to claim 22 said wherein plurality of resolution processors include at least one hyper resolution processor for producing hyper resolution motion analysis.

28. The video encoding device according to claim 1 wherein said digital signal processor comprises:

a DSP controller,

a plurality of processing units, for processing said multiple frame video digital signal, connected to said DSP controller, and

at least one storage unit, wherein each of said processing units is connected to at least one of said at least one storage units,

said DSP controller controlling said plurality of processing units.

29. The video encoding device according to claim 28 wherein each of said processing units is operative to access any storage address of any of said at least one storage unit, connected thereto.

30. The video encoding device according to claim 28 wherein each of said processing units operates according to a different program command.

31. The video encoding device according to claim 28 wherein each of said processing units operates on a different portion of data.